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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/052,671	01/17/2002	Amr M. Mohsen	M-1007-9C US	6141

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EXAMINER
JONES, HUGH M

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,671	MOHSEN, AMR M.	
	Examiner	Art Unit	
	Hugh Jones	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-22 of U. S. Application 10/052,671, filed 1/17/2002 are presented for examination.

Information Disclosure Statement

2. It is noted that there has been litigation on U.S. Patent 5,544,069. The instant application is a continuation of said issued patent and there is a double patenting rejection against said issued patent. However, the outcome of said litigation has not been provided to the Office. It appears that there has been a conclusion to the litigation.

3. In response, please provide current information pertaining to related to any related litigation and result of the litigation of said patent and whether it impacts prosecution of the instant application.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

5. A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

6. Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

7. Claims 1-22 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over patented claims 1-17 of U.S. Patent No. 5,377,124. Claims 1-22 are anticipated by claims 1-17 in that claims 1-17 contain all the limitations of claims 1-22 of the instant application. Claims 1-22 of the instant application therefore are not patentably distinct from the earlier patented claims and as such are unpatentable for obviousness-type double patenting.

Claim Rejections - 35 USC 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

9. Claims 1-22 are rejected under 35 U.S.C. 102(a) as being clearly anticipated by IBM Technical Disclosure (of record in parent application). See pp. 294-299 (especially figs. 6-7). The IBM document discloses interconnected programmable chips on a substrate which are connnected to and configured by another chip or part of a chip. With respect to claims disclosing multiple layers of conductive traces, see pp. 296-297 and fig. 6. With respect to claim limitations concerning discrete elements, see # 5 of page 298.

10. Claims 1-22 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Carter (of record in parent application).

11. Carter discloses reconfigurable logic. See figure 4a. FIGS. 4A illustrates a configurable logic array containing nine configurable logical elements. As shown in FIG. 4A, each CLE of the nine CLEs 40-1 through 40-9 has a plurality of input leads and one or more output leads. Each input lead has a plurality of access junctions each connecting a selected general interconnect lead to the input lead. The access junctions for input lead 2 of CLE 40-7 are labeled A1 through A4 in FIG. 4A. The access junctions for the other input leads are indicated schematically but are not labeled for the sake of clarity. Similarly, each output lead of each CLE has a plurality of access junctions each connecting the output lead to a corresponding one of the general interconnect leads. The access junctions are indicated schematically for each output lead of each CLE in FIG. 4A. The access junctions for the output lead of CLE 40-7 are labeled B1 through B5. The leads in FIG. 4A which are neither input leads nor output leads are called general interconnect leads and the junctions in FIG. 4A which are not access junctions

for input and output leads are called general interconnect junctions. As shown in FIG. 4A, nine logic elements are placed on an integrated circuit chip together with programmable access junctions and a general interconnect structure which comprises general interconnect leads and programmable general interconnect junctions for connecting various leads to other leads. The general interconnect structure includes a set of general interconnect leads and of programmable junctions interconnecting the general interconnect leads having the property that for each general interconnect lead in the general interconnect structure there is a programming of the general interconnect junctions which connects the given general interconnect lead to one or more other leads in the general interconnect structure. Moreover, there is a programming of the junctions (both access and general interconnect) such that for any given output lead of any CLE in the CLA, and for any given input lead of any other CLE in the CLA, there is a programming of the junctions such that the given output lead is connected to the given input lead. An electrical path from a given output lead to a given input lead always contains at least two access junctions and at least a portion of a general interconnect lead. For example, one electrical path from the output lead of CLE 40-8 to the second input lead of CLE 40-9 contains access junctions A7 and B7 and the marked portion P of a general interconnect lead. Typically, an electrical path from an output lead of one CLE to an input lead of another CLE will also contain one or more general interconnect junctions. Each of logic elements 40-1 through 40-9 represents a collection of circuitry such as that shown in FIG. 2 or some similar structure capable of being configured as described above in FIG. 2 to perform any one of a number of logic functions. To

program the circuitry (both the configurable interconnect switches and the configurable logic elements), selected signals are applied to input leads identified as configuration control input leads thereby to generate a desired logical function in each of the logic elements and to interconnect the logic elements as desired. In FIG. 4A, no specific lead has been identified as an input lead for the configuration control signals. However, any particular I/O pad can be selected for this purpose. The configuration control bits can be input into the configurable logic array either in series or in parallel depending upon design considerations where they are typically stored in a programming register (shown in FIG. 5). Alternatively, the configuration control bits may be stored in a memory on chip. In addition, another I/O pad will be used for an input clock signal which is used, inter alia, for the loading of the configuration control signals into the programming register. When the configurable logic array shown in FIG. 4A has been configured, selected output signals of logic elements 40-1 through 40-9 are provided to selected I/O pads. FIG. 4B illustrates the meaning of the junction symbols used in FIG. 4A.

12. Claims 1-22 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Kung et al. (U. S. Patent 4,807,183; of record in parent application) or El Gamal et al. (U. S. Patent 4,873,459 of record in parent application).

13. Kung et al. disclose a programmable interconnection chip for computer system functioanl chips. See abstract; figs. 2-4; col. 1, line 25 to col. 2, line 32; col. 4, lines 5-55.

14. El Gamal et al. disclose a configurable logic circuit which achieves versatility by including a configurable combinational logic element, a configurable storage circuit, and

a configurable output select logic. The input signals to the configurable combinational logic element are input signals to the configurable logic circuit and feedback signals from the storage circuit. The storage circuit may be configured to operate as a D flip flop with or without set and reset inputs, an RS latch, a transparent latch with or without set and reset inputs, or as an edge detector. In conjunction with the combinational logic element, the storage circuit may also operate as a stage of a shift register or counter. The output select logic selects output signals from among the output signals of the combinational logic element and the storage circuit. See figures 4-8.

15. Any inquiry concerning this communication or earlier communications from the examiner should be:

directed to:

Dr. Hugh Jones telephone number (571) 272-3781, Monday-

Thursday 0830 to 0700 ET,

or

the examiner's supervisor, Jean Homere, telephone number (571) 272-3780.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist, telephone number (703) 305-3900.

mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

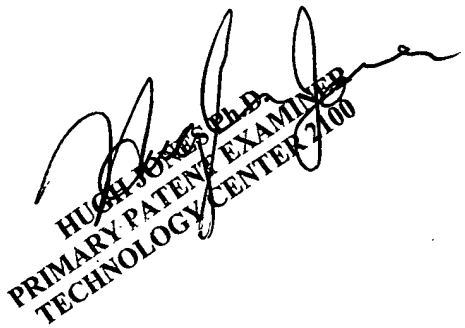
or faxed to:

(703) 308-9051 (for formal communications intended for entry)
or (703) 308-1396 (for informal or draft communications, please label *PROPOSED* or *DRAFT*).

Dr. Hugh Jones

Primary Patent Examiner

July 9, 2005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